Advanced Analog Integrated Circuits

Layout

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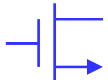
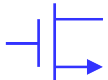


Design & Production Flow

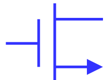
1. Specifications
2. Feasibility & Architecture
3. Circuit Design
4. Layout (DRC)
5. Extraction
6. Verification
   – Layout versus schematics (LVS)
   – Layout parasitic extraction (LPE) → SPICE
7. Fabrication
   – metal dummies …
8. Characterization
9. Production wafer-level test
10. Packaging
11. Packaged die test



Layout Considerations

- Design rules
- Floor plan
- Components
- Matching
- Interference

… and their interactions!



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Design Rules

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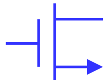
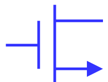
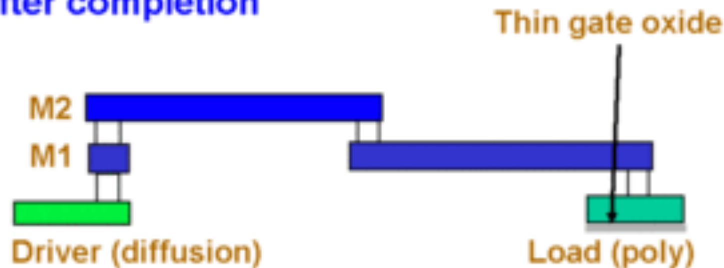


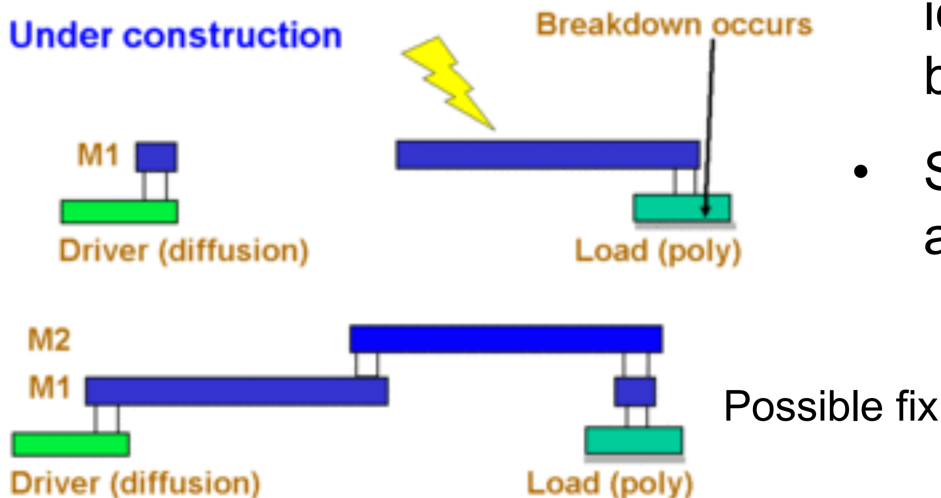
Metal Rules

- Metal density rules
  - CMP → abrasion differences of oxide and metal lead to topology
  - Avoid dummy metal fill
  - Be careful with “exclusion”
    - results in metal thickness uniformity
    - increases mismatch
  - Wide metal rule, e.g. <10μm
- Electromigration: ~1mA/μm
- Maximum (fixed) contact size → arrays



Antenna Rules

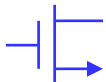




Possible fix

- Load (poly) gate not protected by diffusion diode before M2 deposition
- Charging (during M1 reactive ion etch) can lead to gate breakdown
- Solution: limit metal/gate poly area ratio

https://en.wikipedia.org/wiki/Antenna_effect



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Floor Plan

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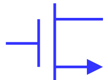


Chip Microphotograph

REFERENCE AND BIAS

PIPELINE BACKEND

LOGIC

STAGE 1

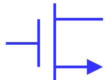
CLK

SHA

B. Murmann and B. E. Boser, "A 12 b 75 Msample/s Pipelined ADC Using Open Loop Residue Amplification," ISSCC 2003.

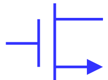
Floor Planning

- Plan overall structure before laying out cells
  - Pin locations
    - Power and ground
    - Keep sensitive inputs away from other signals, clocks
  - Area estimates
  - Organization
    - Cell placements
    - Power distribution
    - Wiring channels
  - Choice of package
    - Size
    - Length, orientation and inductance of bond-wires
- Common mistake
  - Great job laying out lots of small cells
  - Big mess connecting them

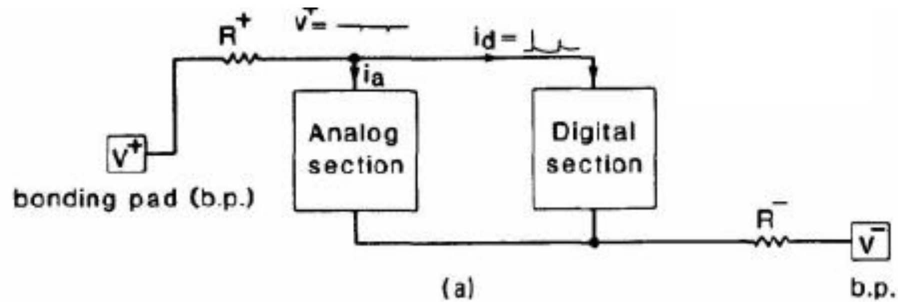


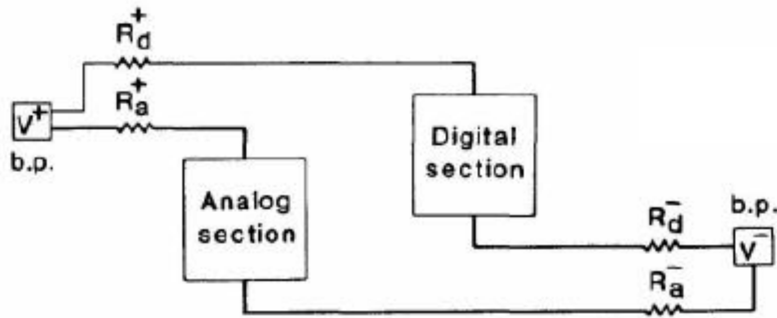
PCB Layout

- Power distribution
  - Decoupling
  - Supply
  - Ground planes
  - Many good references, e.g.
    - Maxim Tutorial 5450: Successful PCB Grounding with Mixed-Signal Chips - Follow the Path of Least Impedance https://www.maximintegrated.com/en/design/design-technology/ground-layout-board-designers.html
- Interconnects to other chips
- Co-design evaluation board with ASIC



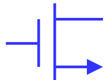
On-Chip Power Routing





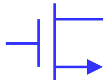
Gregorian & Temes, p. 515

Which is preferable?



Supply Noise

- Typical sources
  - Digital logic
  - Clocks
  - IO pads
- Preventive measures
  - Isolate in space & time
  - On-chip decoupling
  - LVDS I/O
  - Avoid oversizing digital buffers
    - Exacerbates supply noise



Decoupling Network

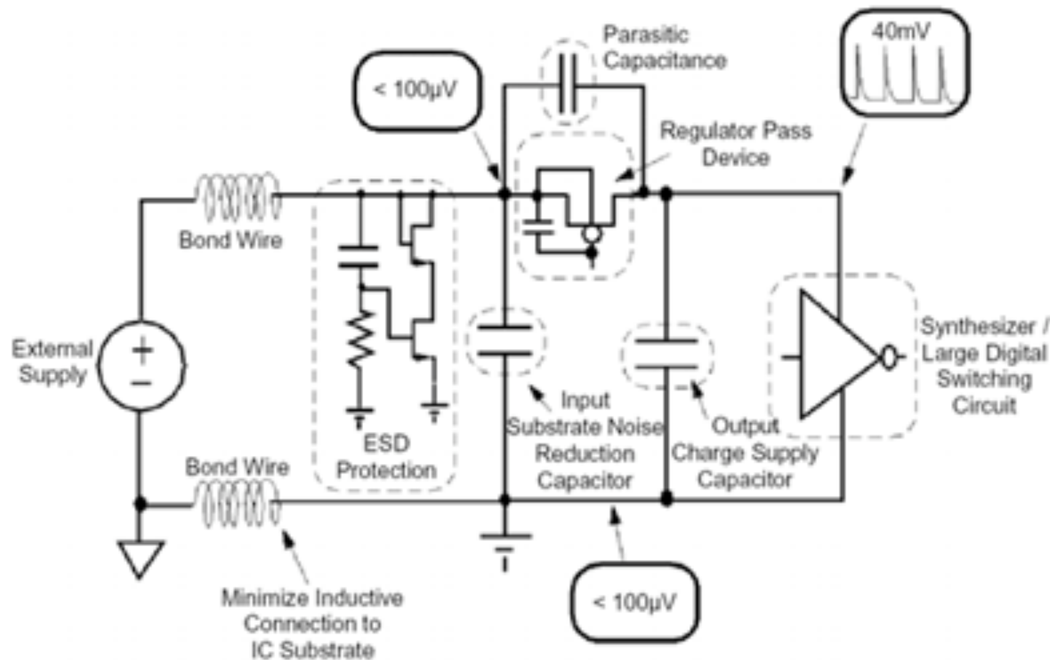
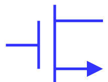
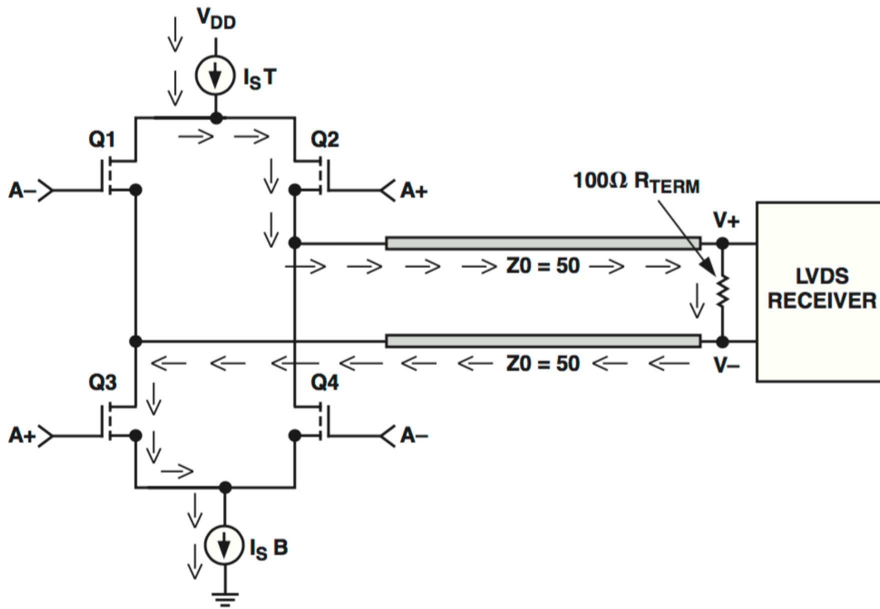


Figure 13: Motorola (ISSCC'02) use of decoupling capacitance to decrease noise.

http://www.commsdesign.com/showArticle.jhtml?articleID=192200561

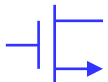


LVDS Outputs



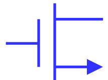
- Well defined current return path
- 2 pins per signal

Ref: ADI application note 586

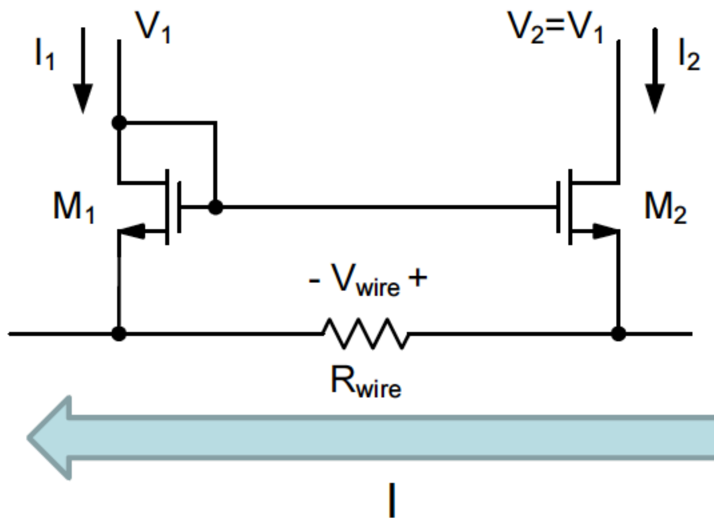


Reference Distribution

- Typically use single band-gap for entire chip
- How distribute to cells?
  a) Bias voltage
  b) Current



IR Drops



- Metal sheet resistance: 50 … 100 mΩ/□
- 10□ → ~1Ω or 1mV/mA
- Use large V*
  - Costs headroom
  - Know most important constraint: dynamic range or matching?

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Components

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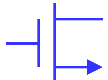
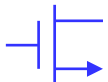


“Parasitics” (sample values)

Layer	Value	T_C ppm/K	V_C ppm/V
Resistance			
n+ diff (no salicide)	50 Ω/□	600	200
p+ diff (no salicide)	80 Ω/□	600	200
n-well	2 kΩ/□	4000	8,000
poly (no salicide)	30 Ω/□	500	100
poly (salicide)	7 Ω/□	200	50
metal 1-4	80 mΩ/□		
metal 5	20 mΩ/□		
Capacitance			
neighboring metals	0.8 fF/μm²		



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Matching

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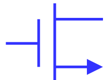
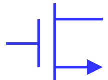


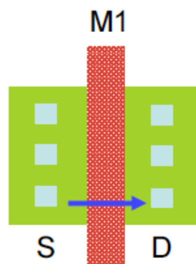
Layout for Matching

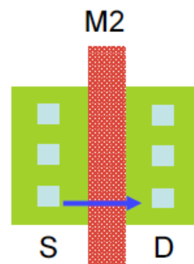
1. Unit elements
   – E.g. equal W and L (use arrays for ratios)
2. Large area
   – Reduces random variations
   – But more susceptible to gradients
   – Beware of increased parasitics
      • Is speed or matching more important?
      • E.g. RF versus ADC
3. Defensive biasing
   – Voltage matching (differential pair): low V*, long L
   – Current matching (mirror): large V*, same V_{DS}



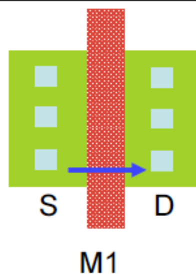
Layout for Matching (cont.)

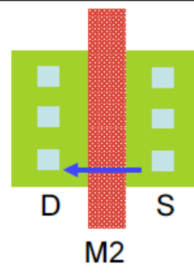
4. Same orientation
   - MOSFETs are nominally symmetrical
   - Actual devices are not
     - Si is not isotropic
     - Implants are not exactly isotropic





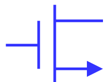
translational symmetry





mirror symmetry

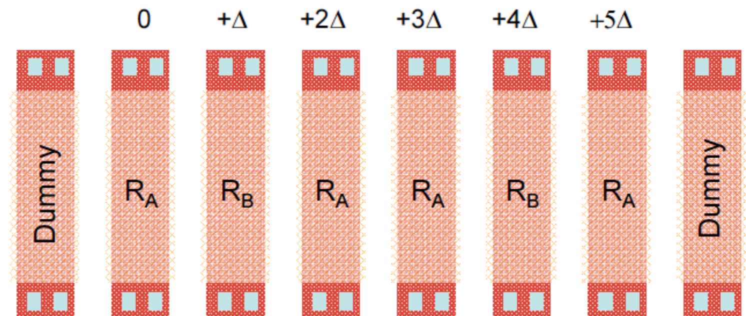
Which is better?



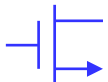
Layout for Matching (cont.)

5. Compact layout
   – Minimize temperature and stress variations
   – Tradeoff with random variations
   – Avoid large aspect ratios
     • E.g. W/L = 180μm/180nm
     • Use fingers → ~ square layout

6. Same vicinity
   – Use dummy elements at edge of array
   – Protects from process non-uniformity, e.g. etch rate
   – Match all layers (including metal)



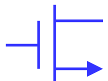
[Su and Murmann]



Layout for Matching (cont.)

7. Stress and proximity effects
   - Package stress
     - Place devices in areas of low stress (typically center of die)
     - At odds with mixed-signal floor plans
   - Local
     - Mostly caused by metal
     - Avoid routing M1 across active area

8. Junctions
   - Keep junction edges (e.g. well) away from transistors (except S/D)
     - At least 2x junction depth
   - Just because DRC rules permit it, minimum spacing is not always best
     - Not all spaces are critical for overall die size

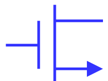


Layout for Matching (cont.)

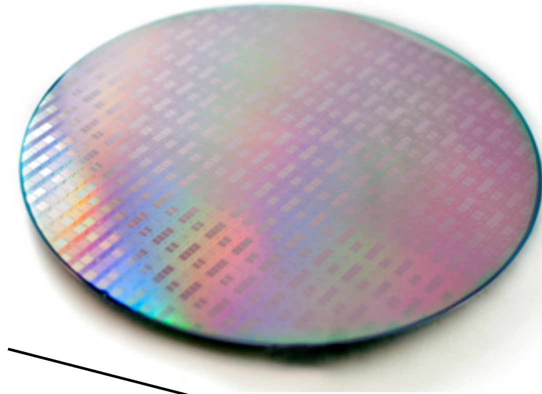
9. Oxide thickness
   – Devices with thinner oxide usually exhibit less mismatch
   – Use minimum oxide thickness, if choice (low voltage devices)

10. Temperature gradients
   – Sources of power dissipation (> ~50mV) result in local heating
   – $\frac{dV_{TH}}{dT} \cong -2\,\mathrm{mV/K}$
   – Keep matched devices away from hot spots
   – Beware of "Temperature memory effect" (thermal τ usually > $1/f_s$)

11. Common centroid layout
   – See following slides



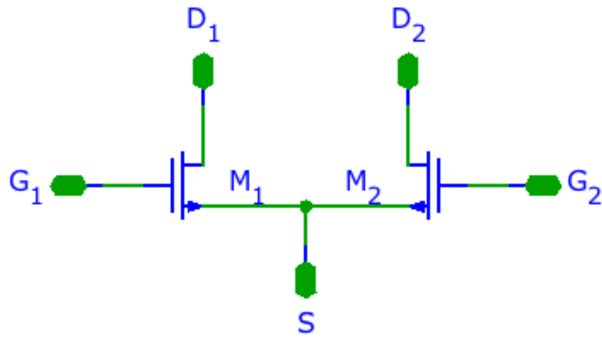
Process Gradients



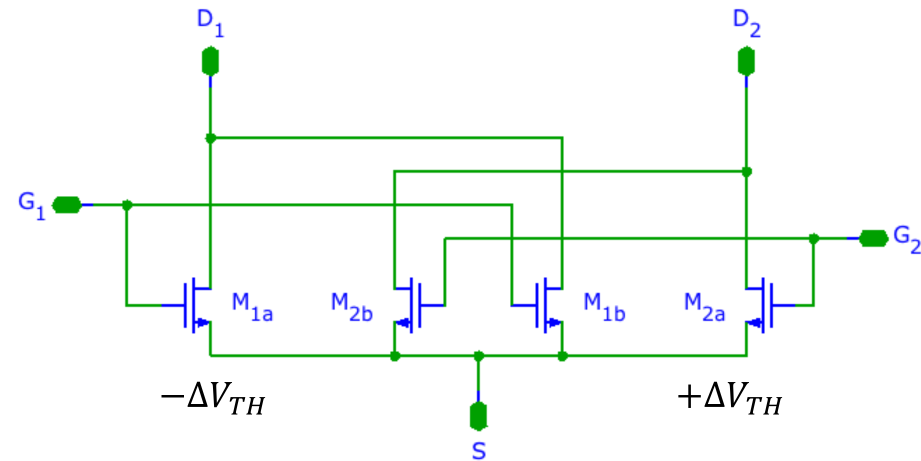
(e.g.) direction of increasing V_{th}

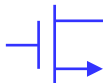
- Parameter variations across wafer
- Typically small, well approximated by linear gradient, at least for devices in close proximity
- Caused by processing artefacts, e.g. etchant concentration higher near the edge

Example: Diff Pair Common Centroid Layout

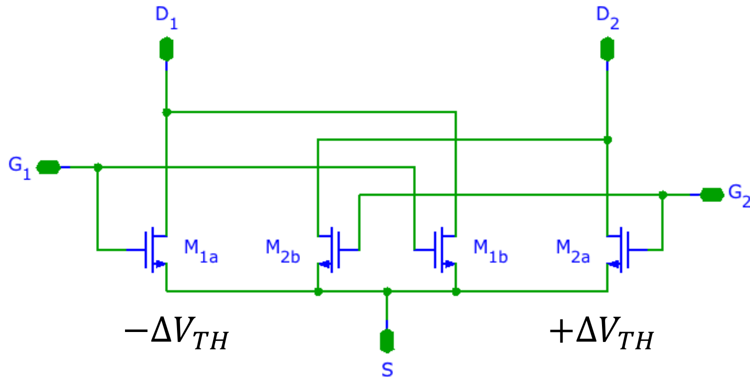


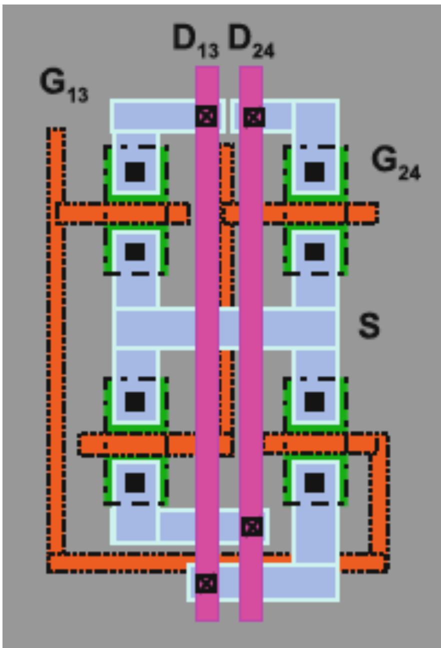
- Linear gradients "average out" in common-centroid layout





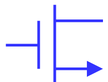
Common Centroid Layout 1



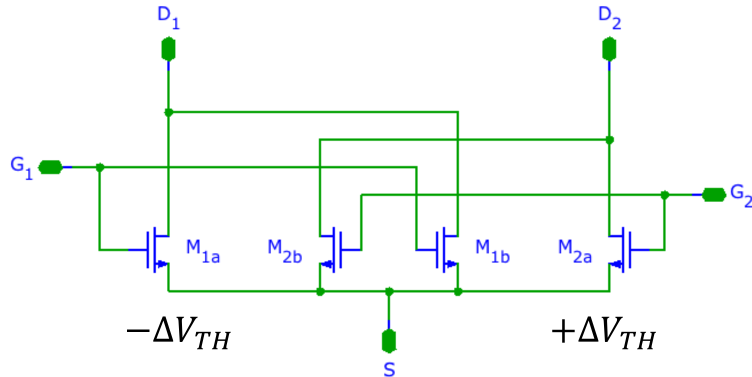


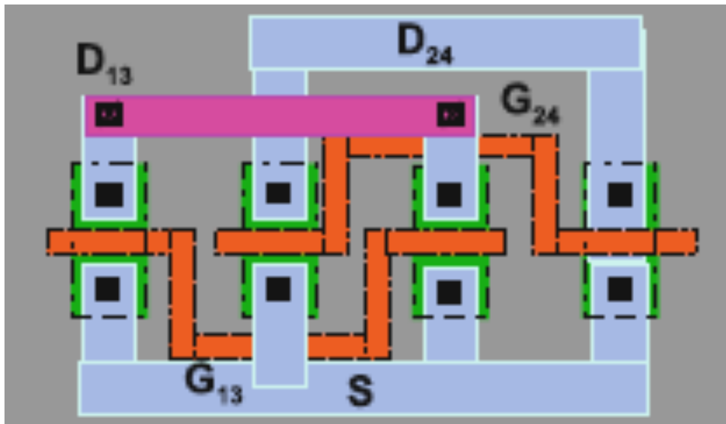
- Lots of possibilities
- "Common-centroid" in horizontal ***and*** vertical direction, should be double good?
- Not really:
  - Imbalanced wiring around transistors
  - Mismatched gate parasitics
  - G_{24} overlaps source, G_{13} does not

Ref: M. Pelgrom et al, "A designer's view on mismatch," Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.



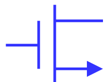
Common Centroid Layout 2





- A better option
- Asymmetry at the drains
  - pull D_{13} farther away from G_{24}?
- Beware of what is to the left and right
  - place dummies as needed

Ref: M. Pelgrom et al, "A designer's view on mismatch," Chapter 13 in Nyquist A/D Converters, Sensors, and Robustness, Springer 2012, pp. 245-67.

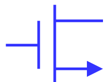


Common Centroid Layout Principles

1. Coincidence:
   - Center of all matched devices coincide

2. Symmetry:
   - X- and Y-axis
   - R's and C's exhibit 1-axis symmetry

3. Dispersion:
   - High dispersion reduces sensitivity to higher order (nonlinear) gradients
   - E.g.
     - ABBAABBA: 2 runs (ABBA) of 2 segments (AB, BA)
     - ABABBABA: 1 run of 2 segments (AB, BA)
     - → ABABBABA has higher dispersion (preferable)



Common Centroid Layout Principles (cont.)

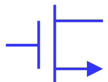
4. Compactness:
   - Approximately square layout
   - 2D patterns
     - Better approximation of square layout
     - Usually higher dispersion possible, e.g.

$_DA_SB_D$
$_DB_SA_D$

$_DA_SB_DB_SA_D$
$_DB_SA_DA_SB_D$

$_DA_SB_DB_SA_D$
$_DB_SA_DA_SB_D$
$_DA_SB_DB_SA_D$
$_DB_SA_DA_SB_D$

5. Orientation:
   - Stress induced mobility variations: several percent error
   - Tilted wafers: ~5% error



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Interference

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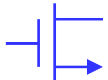
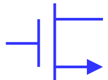


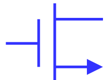
Coupling Mechanisms

- Interconnects
  - Mostly capacitive
  - Mitigation:
    - Distance
    - Shielding (constant potential in-between, e.g. supply or fixed control)
    - Isolation in time (sample at “quiet” moment)
- Package
  - Bondwires
- Supply
- Substrate



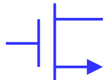
Package

- (Mutual) inductance
- $\Delta V \sim {}^{dI}/_{dt}$
  - Beware of fast transients
  - Test at low temperature (and fast corner wafers)
- Measures:
  - Differential circuits (LVDS IO)
  - Orthogonal bondwires
  - Choose package and pad layout that minimizes length of critical bond wires (supplies and fast signals)

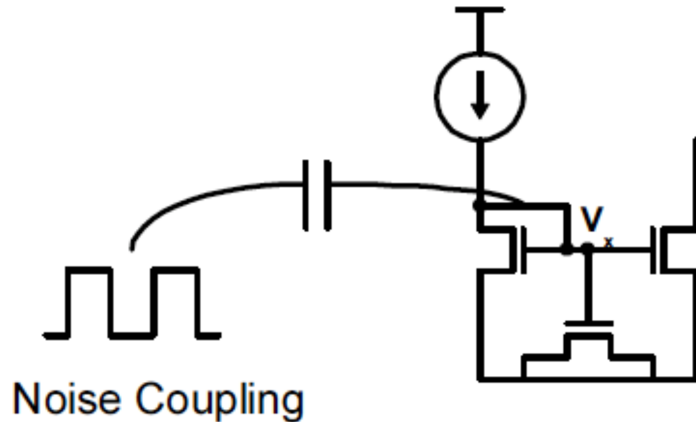


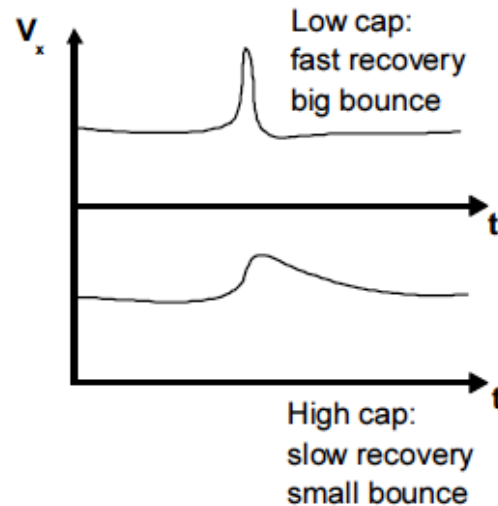
Power Supply

- Separate zones
- Regulator
  - Beware: low output impedance only at low frequencies!
- Decoupling capacitors
  - Key: low impedance (to load)
    - Close
    - Low area return path
  - Choose full equivalent model in simulations
  - Fast and right size is better than big and slow



Capacitive Coupling - Bias

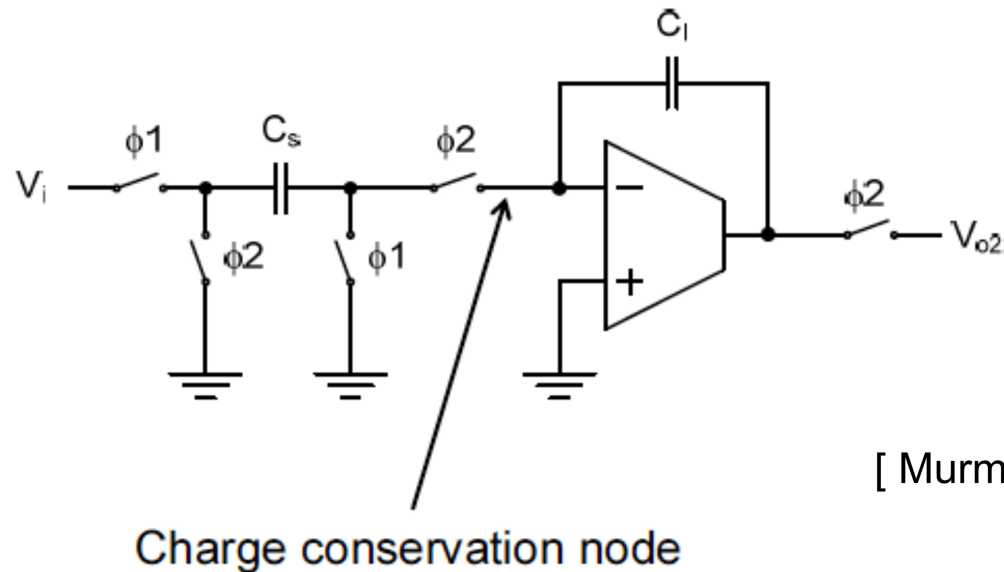




[Murmann]

- Can use decoupling capacitors to reduce the amplitude of noise coupling into bias nodes
- If noise is "deterministic" and occurs at a “don’t care” point in time, you might be better off not decoupling, but making the bias node "fast" (small mirror ratio, no decoupling cap) so it can recover quickly
- Must go for either extreme case: no decoupling or large decoupling

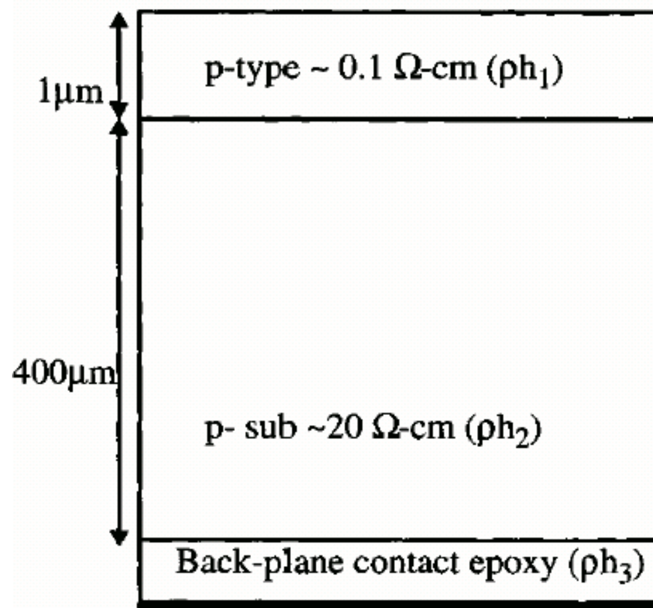
Capacitive Coupling – SC Circuit

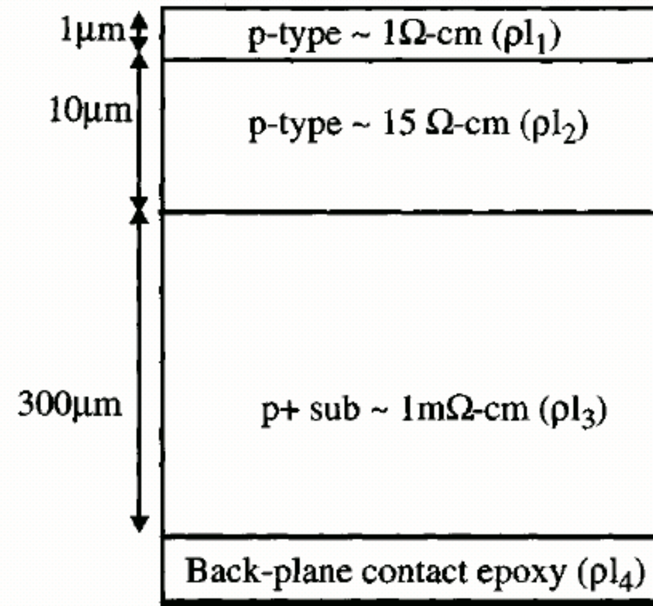


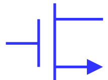
[Murmann]

- Must minimize coupling into charge conservation node
  - Proper placement of “bottom plate” parasitics
  - Substrate shielding

Substrate Types





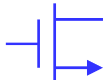


Epitaxial Substrate

Oscilloscope
50 Ω
Ring Oscillator (on chip)
–5 V
–3 V
–5 V
Switching Noise Source
RG 174
Source
Gate
Drain
0.2 pF
N+
N+
P+
7 μm
Current Source Transistor
Substrate Contact
P⁻ Epitaxial Layer (15 Ω-cm)
P+ Channel Stop Implant (1 Ω-cm)
300 μm
P+ Bulk (0.05 Ω-cm)

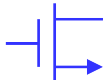
Note:
Lack of backside wafer contact substantially increases coupling!

D. K. Su, M. J. Loinaz, S. Masui, and B. A. Wooley, "Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits," *IEEE Journal of Solid-State Circuits,* vol. 28, pp. 420 - 430, April 1993.



Waveforms

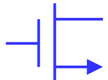
-0.434
-0.436
-0.438
-0.440
-0.442
-0.444
-0.446
V_{out} (V)
0
20
40
60
80
100
120
140
160
Time (ns)
V_{P-P} = 10.7 mV
Settling Time
to within 0.5 mV
= 6.8 ns
1 mV



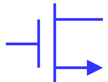
Current flow in Epi-Substrate

Substrate Contacts
NMOS Transistor
Equivalent Drain Diffusion
Substrate Contacts
Epitaxial Layer
P^+ Bulk
Distance (μm)
0
10
20
30
40
50
0 50 100 150 200 250 300 350 400 450
Distance (μm)

- Majority of current flows in low-resistivity wafer
- Coupling is very weak function of distance



Cross-Talk versus Distance



Guard Rings

Peak-to-Peak Noise (mV)

16
14
12
10
8
6
4
2
0

No P+ Guard Ring
With P+ Guard Ring

6-µm distance
22-µm distance
(dedicated package pin)

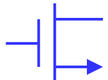
6-µm distance
22-µm distance
(connected to large substrate contact)

Guard Ring Configuration

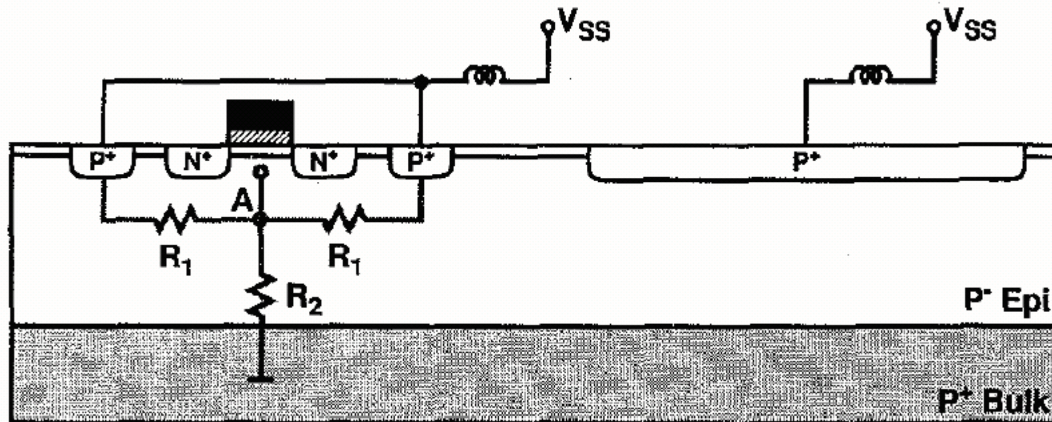
Not much effect

Large guard rings increase coupling!

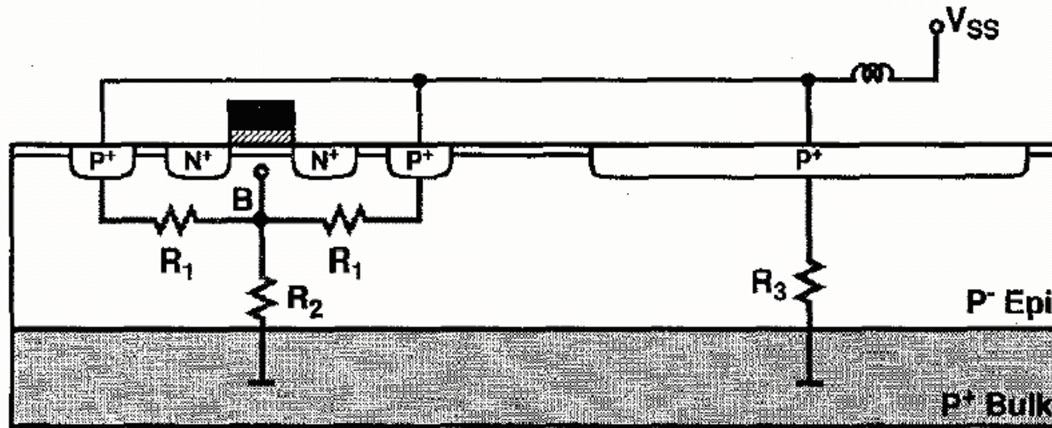
Epi substrate



Model for Guard Ring

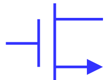


(a)



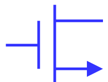
(b)

Shared guard ring contact reduces isolation!

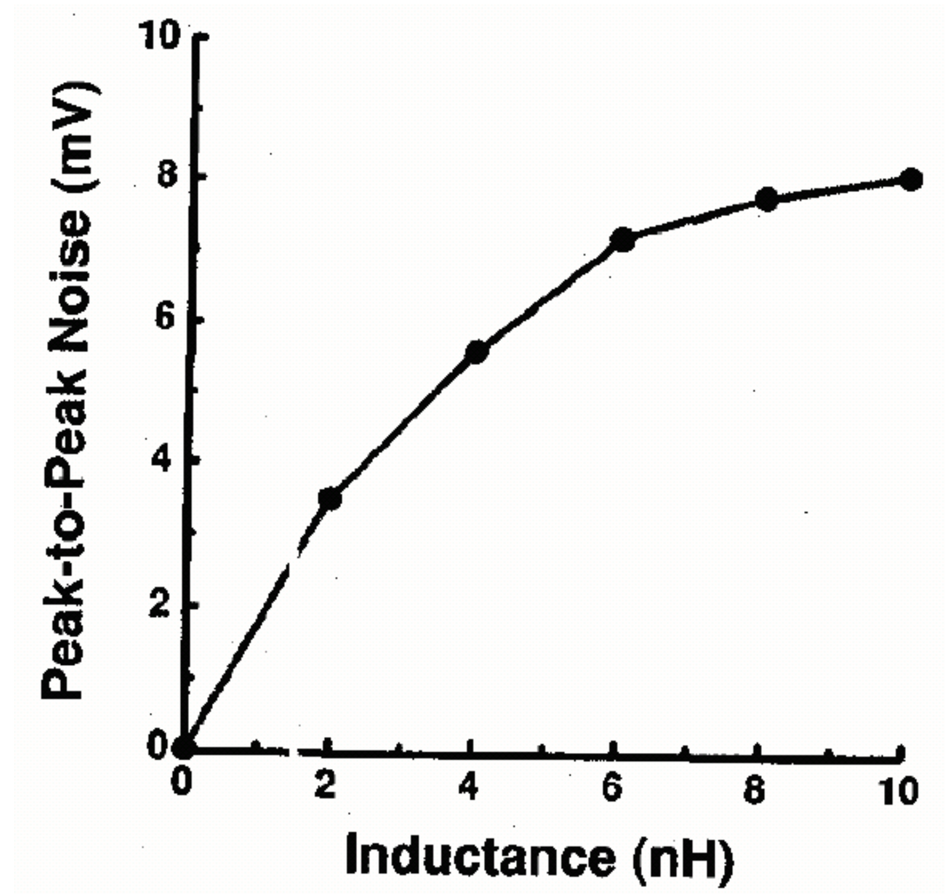


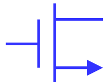
Backside Contact

–3 V
–5 V
L_1
1-ns edge
50Ω
+
V_{out}
-
L_2
L_3
–5 V
(200 µm)
P+
N+
N+
N+
P+
50 µm
d
50 µm
50 µm
Device Structure
P^- Epitaxial Layer
P^+ Channel Stop Implant
(90 µm)
P^+ Bulk
C_1
L_4 (for backside contact only)
–5 V
–5 V



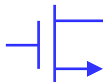
Noise versus Backside Contact Inductance





Summary for Epi-Substrate

- Substrate closely modeled by ”single equipotential node”
- Most effective approach to minimize coupling”
  - Low resistance and inductance backside contact
- Guard rings
  - Limited effect
  - Beware of “telephone effect”
    - Use dedicated guard ring potential

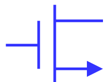


Current in High Resistivity Substrate

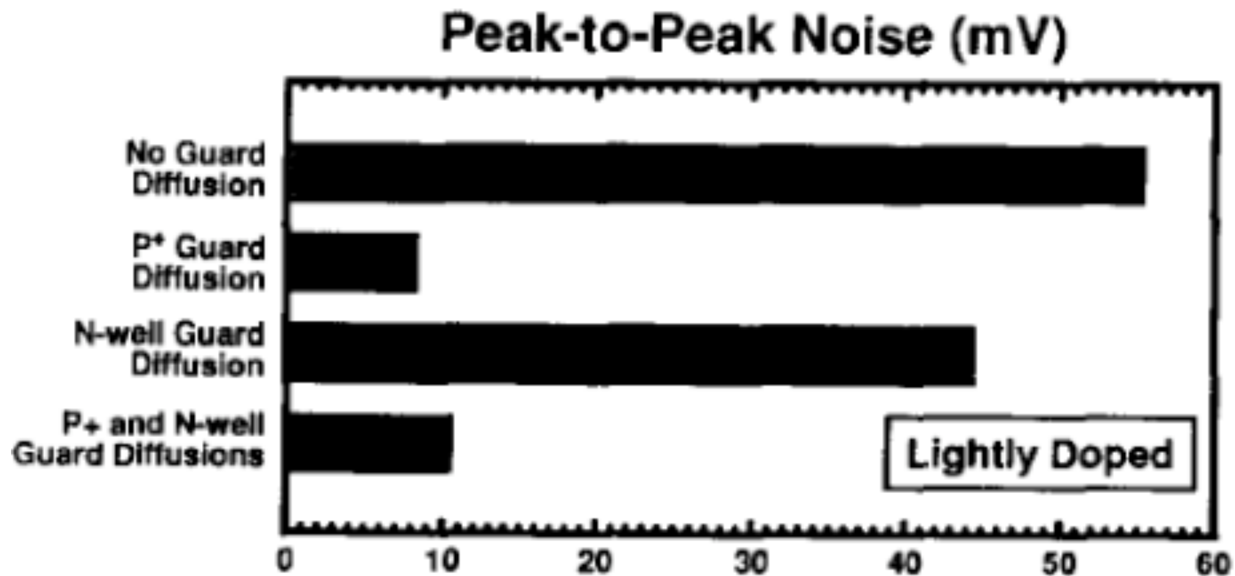
Substrate Contact
NMOS Transistor
Equivalent Drain Diffusion
Substrate Contact
Distance (μm)
0 10 20 30 40 50
0 50 100 150 200 250 300 350 400 450
Distance (μm)

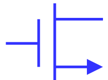
Strongly affected by surface potential

Suggests guard ring should be effective



Guard Rings





Example

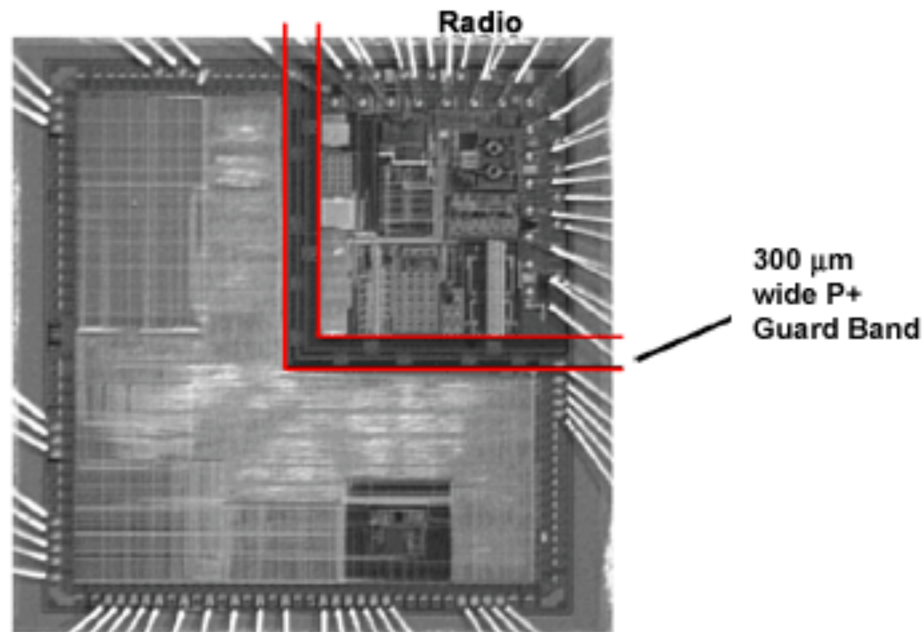


Figure 7: Ericsson single-chip Bluetooth design with a 300-micron-wide, guard band isolation.

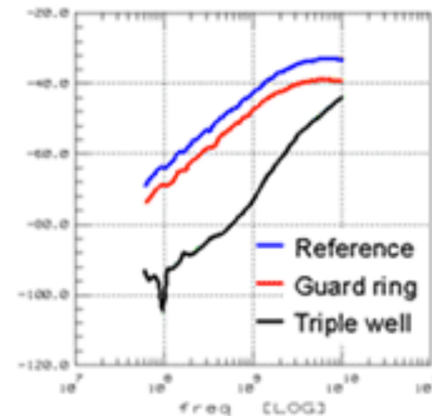
http://www.commsdesign.com/showArticle.jhtml?articleID=192200561

Deep N-Well

Process technology Hip7lp
Compatible with TSMC

Gate length L*poly*	0.13µm
Single gate Ox	30A
Dual gate Ox	50A
Supply voltage	1.6 to 3.0V
Metal	5 layer Cu
Substrate	P+
Nwell resistors	700 ohm/sq.
Salicided Poly res.	7.0 ohm/sq.
Metal Cap	0.8 fF/um^2

Benefits of IPW Isolation



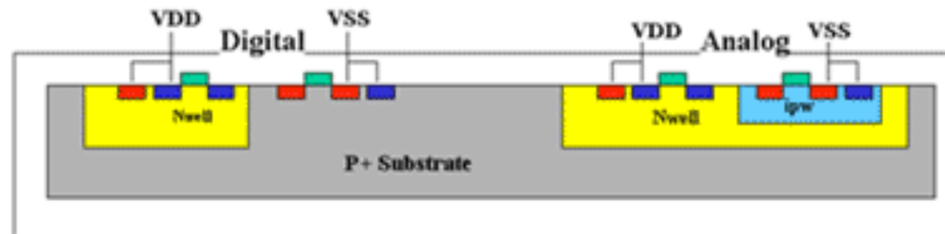
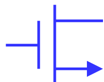


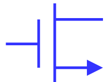
Figure 3: Motorola (ISSCC'02) triple-well example showing approximately 20 dB of additional isolation. The top curve is with no triple well or guard ring. The middle curve shows the isolation added by a guard ring, while the bottom curve is the triple-well isolation.

http://www.commsdesign.com/showArticle.jhtml?articleID=192200561



Summary for Lightly Doped Substrate

- Distance and guard rings reduce coupling significantly
- But beware of injecting noise through guard rings



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